ALLWINNER

V5 V100

4K@30fps
high-level camera solution

Overview

As a specific SoC in video encoding industry designed for HD IP Camera, the V5 V100 integrates dual-channel independent ISP, and uses the latest H.265 video compression encoder in the industry that supports encoding of multiple streams. Integrated intelligent analysis accelerate engine supports various intelligent analysis applications such as intelligent motion detection, perimeter protection, and face detection. By independent image processing engine, the V5 V100 supports Lens distortion correction, Fisheye and PTZ calibration. It also supports real-time stitching for two-channel images (panoramic 360°, wide angle 180°), and picture rotation by 90°or 270°.The V5 V100 integrates various sensor interfaces including HiSPi, Sub-LVDS, MIPI, Parallel interface, as well as advanced low-power technology and architecture design, which significantly reduces the BOM cost of the HD IP camera based on the V5 V100. The Allwinner SDK features high stability and ease of use, supports rapid mass production, and facilitates system layout of IP Camera and 4K action cameras.

Highlights

- Quad-Core ARM Cortex-A7, frequency up to 1.5GHz, with high performance of extending capability.

- Integrated intelligent analysis accelerate engine, support various intelligent analysis applications such as motion detection, perimeter defense，video diagnosis and face detection.

- Support 4K30fps H.264/H.265 encoding and Real-time multi-stream encoding capability : 3840x2160@30fps+VGA@30fps+3840x2160@1fps picture capture.

- Integrated dual-channel independent ISP, support dual-channel Sensor input and recording.

- High system integration, with a wide range of connectivity and interfaces, including sensor interface such as HiSPi/Sub-LVDS/MIPI/Parallel, various output interfaces such as RGB/LVDS/MIPI/HDMI, and as well as audio codec，GMAC etc.

Feature List

Processor Core

- Quad-Core Cortex A7@1.5GHz
- Neon acceleration, integrated FPU

Video Encoding/Decoding Performance

- H.264 BP/MP/HP，H.265 Main Profile encoding
- I/P Frame，Smart P frame reference
- MJPEG/JPEG baseline encoding
- Real-time multi-stream H.264/H.265 encoding capability:-3840x2160@30fps+VGA@30fps+3840x2160@1fps snapshot
- Maximum JPEG snapshot performance of 3840x2160@30fps
- Maximum H265/H264/MJEPG decoding performance of 3840x2160@30fps
- CBR，VBR modes
- Encoding of eight ROIs
- Support Frame Buffer Uncompression

Intelligent Video Analysis

- Integrated AIE, supporting various intelligent analysis applications such as motion detection, perimeter defense，video diagnosis and face detection

Audio Interface

- Integrated audio CODEC supporting 20-bit audio inputs and outputs
- I2S interface for connecting to an external audio CODEC
- Dual-channel differential MIC inputs for reducing background noises

Video Interface

Input

- Two sensor input，Main input support 4xLane MIPI/12xLane Sub-LVDS/4xLane HiSPi interface，second input support 4xLane MIPI/8xLane Sub-LVDS/4xLane HiSPi interface
- Compatibility with mainstream HD CMOS sensors provided by Sony, Aptina, OmniVision, and Panasonic
- Support BT.601, BT.656, or BT.1120 interface

Output

- One PAL/NTSC output for automatic load detection
- One BT.1120/BT.656 output interface
- One MIPI DSI output，Maximum support 1080P60fps
- One RGB/LVDS output

Audio Encoding/Decoding

- Voice encoding/decoding complying with multiple protocols by using software
- Compliance with the G.711, G.726 and ADPCM protocols
- Audio 3A functions (AEC, ANR, and ALC)

Peripheral Interfaces

- POR，External reset input
- Internal RTC，Integrated 4-channel ADC
- Six UART interfaces，Eight PWM interfaces
- One USB2.0 OTG，One USB2.0 Host
- RGMII/RMII in 10/100 Mbit/s full-/half-duplex mode and1000Mbit/s full-duplex mode

ISP

• 2-channel independent ISP processing, ISP1 Maximum support 4224x3168@30fps, ISP2 Maximum support 3264x2560@30fps
• Adjustable 3A functions (AE, AWB, and AF)
• Highlight compensation, backlight compensation, gamma correction, and color enhancement
• Defect pixel correction, 2D/3D denoising
• Support Sensor Build-In WDR、2F - Frame base/Line base WDR、Local Tone mapping
• Support 4-channel 1/64～1x scale output, include 2-channel support Frame Buffer compression
• OSD overlaying of eight regions before encoding
• Picture mirroring and flipping
• ISP tuning tools for the PC

Video and Graphics Processing

• Lens distortion correction and fisheye correction
• Binocular stitching (360° panorama, 180° wide angle)
• Picture rotation by 90° or 270°

Graphics Display

• 2-Channel Video layer, Maximum support 4K@30fps
• 2-Channel UI layer, Maximum support 1080P@30fps
• 2-Channel Video layer overlying 2-Channel UI layer
• Support Screen color enhance

Security Engine

• AES, DES, and 3DES encryption and decryption algorithms implemented by using hardware
• RSA1024/2048/4096 signature verification algorithm implemented by using hardware
• Hash-SHA1/256 and HMAC_SHA1/256 tamper proofing algorithms implemented by using hardware
• Integrated 1.5Kbit Efuse storage space

External Memory Interfaces

• DDR3/DDR3L/LPDDR3/ DDR2/LPDDR2 interface
- 32bit LPDDR3 with the maximum frequency of 667 MHz
- 32bit DDR3/DDR3L with the maximum frequency of 800 MHz
• SPI NOR flash interface, Maximum capacity of 32 MB
- 1-/2-/4-wire mode
- 3-byte or 4-byte address mode
• SPI NAND flash interface, maximum capacity of 512 MB
• eMMC 5.0 interface, maximum capacity of 2 TB
• NAND flash interface, Components with 8 GB or larger capacity
- 8-bit data width
－4-/8-/24-/40-/64-/80-bit ECC
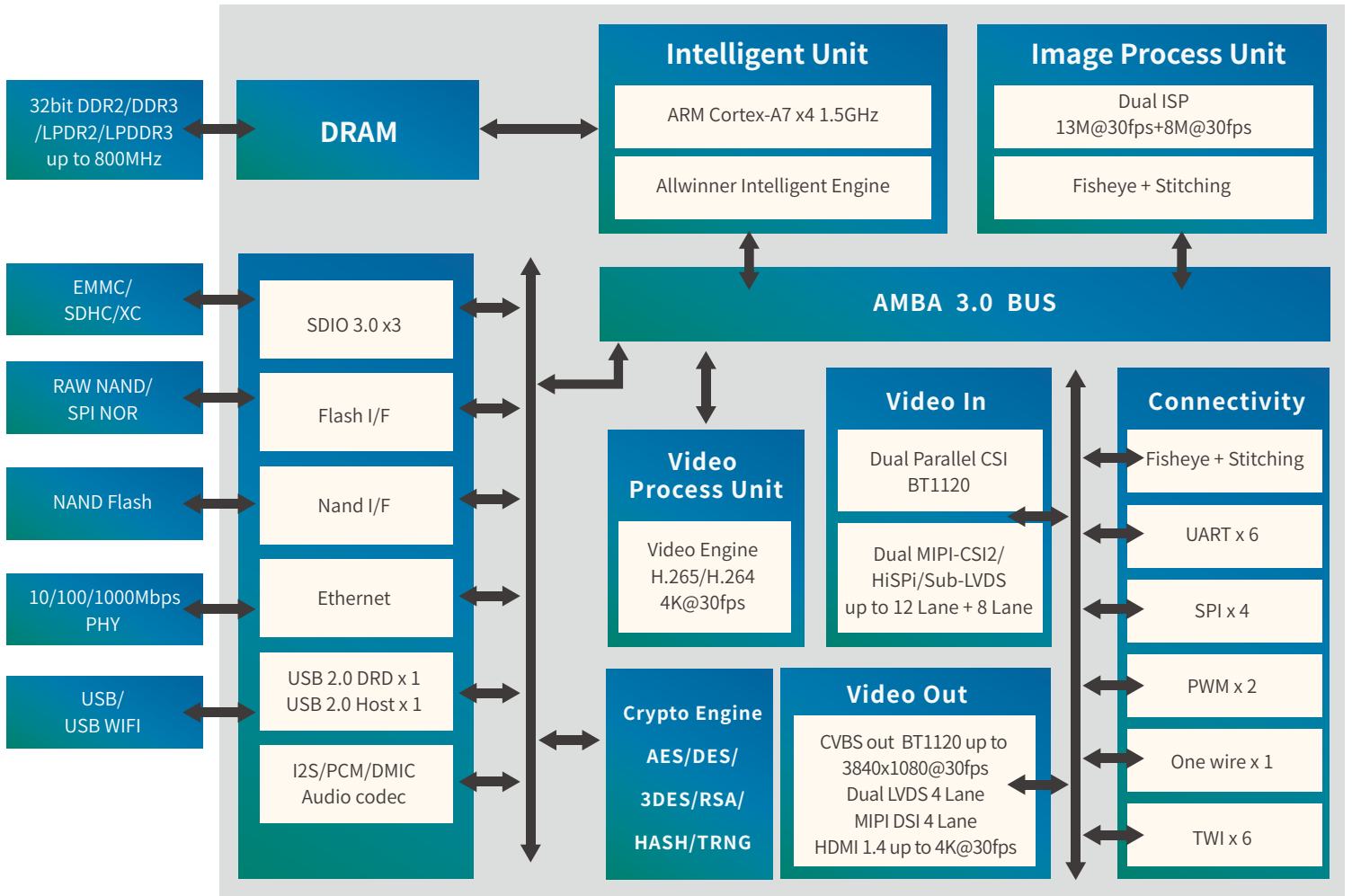• Booting from the SPI NOR flash, SPI NAND flash, or NAND flash

Physical Specifications

• Power consumption
- TBD
- Multi-level power saving mode
• Operating voltages
- 0.9 V core voltage
- 3.3 V I/O voltage and 3.6 V margin voltage
- 1.5 V, or 1.2V DDR3/3L/LPDDR3 SDRAM interface voltage
• Package
- RoHS, TFBGA
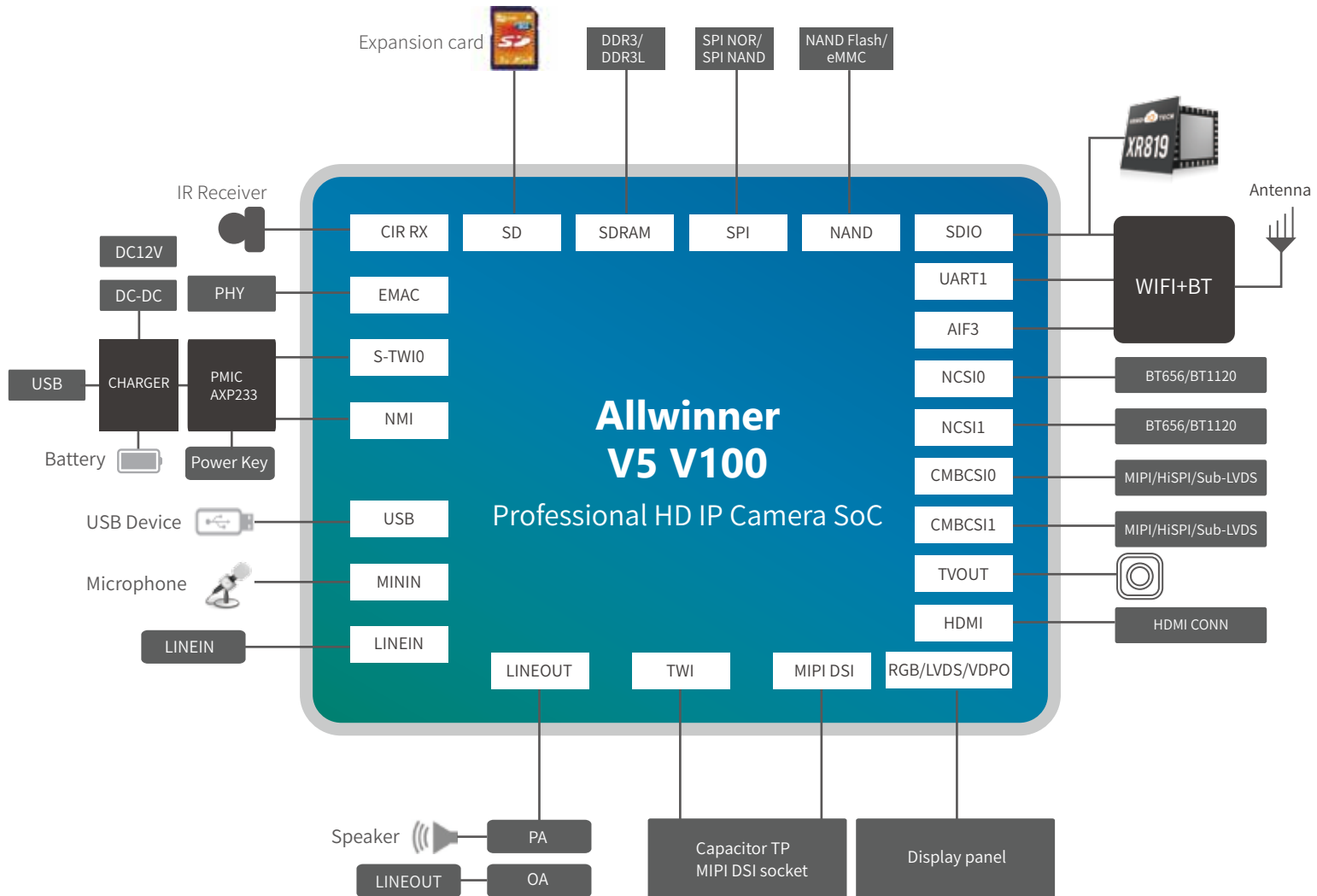- Body size of 17mm x 17mm, Lead pitch of 0.65mm

SDK

• Linux-4.4-based SDK

Block Diagram

Block	Contents
Intelligent Unit	ARM Cortex-A7 x4 1.5GHz
	Allwinner Intelligent Engine

Block	Contents
Image Process Unit	Dual ISP 13M@30fps+8M@30fps
	Fisheye + Stitching

32bit DDR2/DDR3 /LPDR2/LPDDR3 up to 800MHz → **DRAM**

AMBA 3.0 BUS

- EMMC/ SDHC/XC → SDIO 3.0 x3
- RAW NAND/ SPI NOR → Flash I/F
- NAND Flash → Nand I/F
- 10/100/1000Mbps PHY → Ethernet
- USB/ USB WIFI → USB 2.0 DRD x 1 / USB 2.0 Host x 1
- I2S/PCM/DMIC Audio codec

Video Process Unit
Video Engine H.265/H.264 4K@30fps

Video In
Dual Parallel CSI BT1120
Dual MIPI-CSI2/ HiSPi/Sub-LVDS up to 12 Lane + 8 Lane

Connectivity
- Fisheye + Stitching
- UART x 6
- SPI x 4
- PWM x 2
- One wire x 1
- TWI x 6

Crypto Engine
AES/DES/
3DES/RSA/
HASH/TRNG

Video Out
CVBS out BT1120 up to 3840x1080@30fps
Dual LVDS 4 Lane
MIPI DSI 4 Lane
HDMI 1.4 up to 4K@30fps

Application Diagram

Expansion card

DDR3/DDR3L

SPI NOR/SPI NAND

NAND Flash/eMMC

XR819

Antenna

IR Receiver

| CIR RX | SD | SDRAM | SPI | NAND | SDIO |

DC12V

PHY

| EMAC | | UART1 | WIFI+BT |

DC-DC

| AIF3 |

USB

CHARGER

PMIC AXP233

| S-TWI0 |

| NCSI0 | BT656/BT1120 |

Battery

Power Key

| NMI |

| NCSI1 | BT656/BT1120 |

Allwinner V5 V100
Professional HD IP Camera SoC

| CMBCSI0 | MIPI/HiSPI/Sub-LVDS |

USB Device

| USB |

| CMBCSI1 | MIPI/HiSPI/Sub-LVDS |

Microphone

| MININ |

| TVOUT |

LINEIN

| LINEIN |

| HDMI | HDMI CONN |

| LINEOUT | TWI | MIPI DSI | RGB/LVDS/VDPO |

Speaker

| PA |

Capacitor TP MIPI DSI socket

Display panel

LINEOUT

| OA |

V5 DV100

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• Compatibility with mainstream HD CMOS sensors provided by Sony, Aptina, OmniVision, and Panasonic

Output
• One PAL/NTSC output for automatic load detection
• One BT.1120/BT.656 output interface
• One HDMI output，Maximum support 4K30fps
• One MIPI DSI output，Maximum support 1080P60fps
• One RGB/LVDS output

Audio Encoding/Decoding
• Voice encoding/decoding complying with multiple protocols by using software
• Compliance with the G.711, G.726 and ADPCM protocols
• Audio 3A functions (AEC, ANR, and ALC)

Peripheral Interfaces
• POR，External reset input
• Internal RTC，Integrated 4-channel ADC
• Six UART interfaces，Eight PWM interfaces
• One USB2.0 OTG，One USB2.0 Host
• RGMII/RMII in 10/100 Mbit/s full-/half-duplex mode and1000Mbit/s full-duplex mode

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- 1-/2-/4-wire mode

- 3-byte or 4-byte address mode

• SPI NAND flash interface, maximum capacity of 512 MB

• eMMC 5.0 interface, maximum capacity of 2 TB

• NAND flash interface，Components with 8 GB or larger capacity

- 8-bit data width

- 4-/8-/24-/40-/64-/80-bit ECC

• Booting from the SPI NOR flash, SPI NAND flash, or NAND flash

Peripheral Interfaces

• POR，External reset input

• Internal RTC，Integrated 4-channel ADC

• Six UART interfaces，Eight PWM interfaces

• Three SD3.0/SDIO3.0 interfaces

• One USB2.0 OTG，One USB2.0 Host

• RGMII/RMII in 10/100 Mbit/s full-/half-duplex mode and1000Mbit/s full-duplex mode
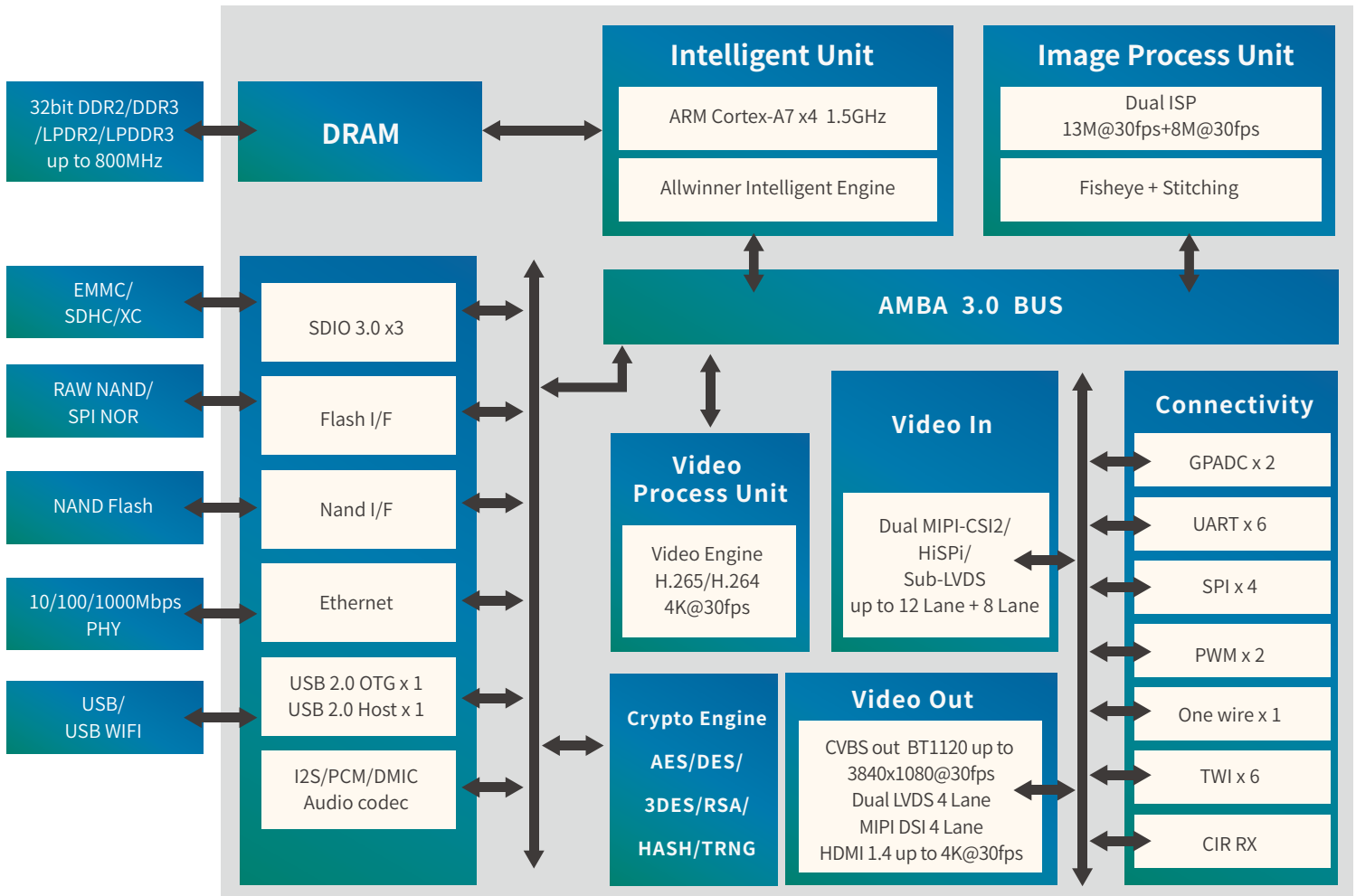
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• Power consumption

- TBD

- Multi-level power saving mode

• Operating voltages

- 0.9 V core voltage

- 3.3 V I/O voltage and 3.6 V margin voltage

- 1.5 V, or 1.2V DDR3/3L/LPDDR3 SDRAM interface

voltage

Package

- RoHS，TFBGA

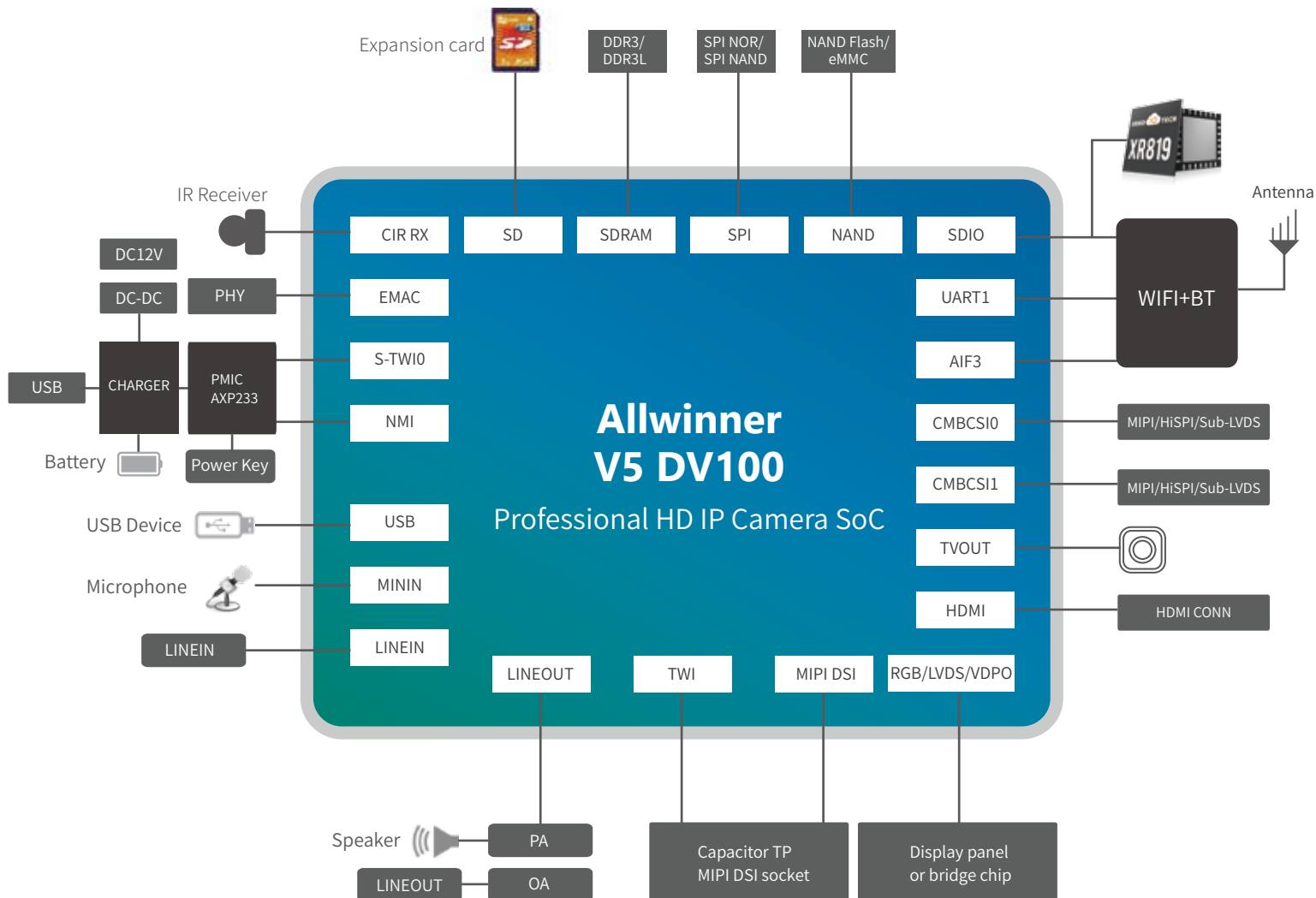- Body size of 14mm x 14mm，Lead pitch of 0.5mm

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• RSA1024/2048/4096 signature verification algorithm implemented by using hardware

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• Integrated 1.5Kbit Efuse storage space

Block Diagram

Application Diagram

Expansion card · DDR3/DDR3L · SPI NOR/SPI NAND · NAND Flash/eMMC · XR819 · Antenna

CIR RX	SD	SDRAM	SPI	NAND	SDIO
EMAC					UART1
S-TWI0					AIF3
NMI					CMBCSI0
					CMBCSI1
USB					TVOUT
MININ					HDMI
LINEIN					

Allwinner V5 DV100
Professional HD IP Camera SoC

IR Receiver · DC12V · DC-DC · PHY · USB · CHARGER · PMIC AXP233 · Battery · Power Key · USB Device · Microphone · LINEIN

WIFI+BT

MIPI/HiSPI/Sub-LVDS · MIPI/HiSPI/Sub-LVDS · HDMI CONN

LINEOUT	TWI	MIPI DSI	RGB/LVDS/VDPO

Speaker · PA · LINEOUT · OA · Capacitor TP MIPI DSI socket · Display panel or bridge chip